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There are known magnetic-core decoder circuits with square hysteresis loops and transistors (decoding matrices) which contain a receiving storage shift register. A disadvantage of these decoder circuits, which require $n2^n$ magnetic cores and the same number of amplifier triodes (n is the number of bits in the code to be decoded), is the fact that they are multielement circuits and must have at the input an additional device for obtaining the inverse code, which fills the zeros in the direct code.

The proposed decoder circuit differs from these in that, in order to decrease the number of circuit elements, decoding is accomplished in the receiving storage shift register itself; this is a magnetic-core register with a square hysteresis loop. For this purpose, on each anchor ring of the shift register, besides the main windings (input, output and time), are placed decoding windings, to which transistors are connected, the bases of which are connected in series with the decoding windings and the "one" generator windings. The decoding principle is based upon a comparison of the voltage induced in the decoding windings at the instant of switching the anchor rings

by the cadence pulses with the reference voltage, which is obtained from the "one" generator (the latter would fulfill the role of a device for obtaining the inverse code). The number of decoding windings is determined by the number of decimal outputs.

The schematic of the proposed three-digit storage shift register-decoder is shown in the Figure. The shift register is made in a single-cycle circuit with a controllable discharge loop.

Let information with code 011 enter input 1 of the register. Then, upon the arrival of the first pulse of the given code (code pulses follow between cadence pulses), anchor ring 2 is switched to state "1". With the arrival of a cadence pulse, which passes through the loop of series-connected windings 3, this anchor ring switches to state "0", and in its output winding 4 a voltage is generated of polarity such that, by passing through diode 5 of delay loop 6, it charges capacitor 7. The discharge loop of the capacitor at this instant is opened by switch loop 8. By the end of the passage of the cadence pulse, the switch loop closes and capacitor 7 is discharged by input winding 9 of the next anchor ring 10. Thus, under the influence of a cadence pulse, the information is shifted one step. Therefore, at the moment of arrival of the second cadence pulse, anchor rings 10 and 11 will be switched to state "1".

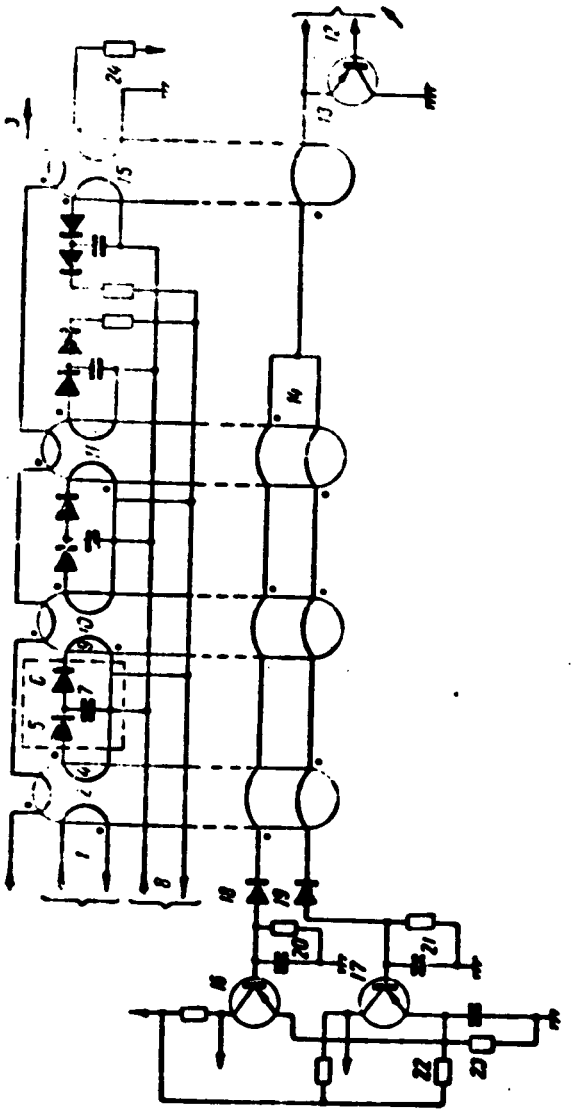
With the arrival of the third cadence pulse of the signal from cycle distributor 12 (with magnetic cores and controllable from the same cadence-pulse source) triode 13 is opened. At this same moment, the voltage generated in series-connected decoding windings 14 of the storage shift register is compared with the voltage generated in reference anchor ring 15. From the circuit it is obvious that, for this example (information with 011), the output control voltage (of negative polarity) appears only in the upper series of decoding

windings (at the input of triode 16), just as a resultant voltage of positive polarity appears in the other series of windings. Amplifier triode 17 does not react to this latter voltage.

Diodes 18 and 19 serve to prevent the opening of amplifier triodes 16 and 17 from equalizing currents at the moment the information entering the decoder moves along the shift register. Capacitors 20 and 21 are for blocking the imputs of the amplifier stages from pulse noise generated at the moment of decoding, due to an inaccurate coincidence of the durations of pulses generated in the decoding windings and in the windings of the reference anchor ring. In addition, these noise pulses in the amplifier stages are limited by a positive automatic bias fed to the bases of the triodes from a voltage divider consisting of resistors 22 and 23. Adjustment of the circuit comes down to selection of the voltage in the windings of the reference anchor ring due to the change in the magnetizing current by resistor 24 and the change in the automatic-bias voltage to the amplifier stages by resistor 22.

Object of the Invention

The magnetic-core shift register-decoder with a square hysteresis loop and transistors is distinguished by the fact that, in order to decrease the number of circuit elements, decoding windings (whose number is equal to the number of decoder outputs) are placed on each magnetic core; to these windings are connected transistors whose bases are connected in series with the decoding windings and the winding of the "one" generator, which serve to add the induced voltages when decoding.



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